REMARKS/ARGUMENTS

Claims 1-90 are pending. Claims 45-51 have been withdrawn from consideration, and have been cancelled without prejudice. Claims 1-4, 16-28, 52, 53, 60-62, 64-66, 68-70, 73-77, 79, 82 and 83 have been rejected. Claims 5-15, 29-36, 54-59, 63, 67, 71, 72, 78, 80, 81, 84 and 85 have been objected to. Claims 37-44 have been allowed. Claims 1-44 and 52-83 have been amended. Claims 86-90 have been added.

The preambles of Claims 1-44 and 52-85 have been amended merely for clarification. No new matter has been added.

Claims 1 and 22 have been objected to because of various informalities. Claims 1 and 22 have been amended in view of the Examiner's comments. Withdrawal of the objection is respectfully requested.

Claims 1-4 have been rejected under 35 U.S.C. § 102(e) as being anticipated by *Abedifard et al.* (U.S. Patent No. 6,657,913).

Claim 1 has been amended merely to overcome the informalities of the objection described above.

As understood *Abedifard* at best merely discloses a memory device 100 that includes an array of memory cells 102 that are arranged in addressable banks, such as memory banks 104, 106, 108 and 110. ('913 Patent, col. 5, lns. 7-22.) Figure 8 of *Abedifard* shows a memory bank 800 with four memory sectors 400. Each memory sector 400 has four memory blocks and 4,096 sense amplifiers. For example, a section 810_0 is connected to a sense amplifier and multiplexer (SA&MUX). ('913 Patent, col. 10, lns. 52-64.)

Abedifard does not disclose or even suggest a first sensing circuit to detect content in selected memory cells of a first plurality of memory cells using a first sensing mode and a second sensing circuit to detect content of selected memory cells of a second plurality of memory cells using a second sensing mode as recited in Claim 1. As an illustrative embodiment of the sensing modes recited in Claim 1, the first sensing mode may be current mode sensing and the second sensing mode may be voltage mode sensing. The Office Action is silent as to where the *Abedifard* patent describes first and second sensing modes. The Examiner is respectfully reminded of the provisions of 37 CFR §1.104(c)(2) (cited in MPEP §706):

> "When a reference is complex or shows or describes inventions other than that claimed by the Applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified."

Further, as stated in MPEP §707:

> "In accordance with the patent statute, 'Whenever, on examination, any claim for a patent is rejected or any objection . . . made,' notification of the reasons for rejection and/or objection together with such information and references as may be useful in judging the propriety of continuing the prosecution (35 U.S.C. 132) should be given."

Abedifard does not disclose or even suggest first and second sensing modes nor first and second sensing circuits using first and second sensing modes, respectively, as recited in Claim 1. Lacking at least this claim feature, *Abedifard* cannot render claim 1 unpatentable. Therefore, it is respectfully submitted that claim 1 is patentable over the references of record.

Claim 2 recites "the first and second plurality of memory cells are arranged in segments." It is asserted in the Office Action that sectors 400_{0-3} are segments. Applicant respectfully submits that the sectors 400 of *Abedifard* are not the segments recited in claim 2. Applicant notes that the specification discloses several embodiments of segmented arrays in paragraph 0057. The sectors 400 of *Abedifard* are not the segments of memory cells disclosed in the specification or recited in Claim 2. Lacking at least this claim feature, *Abedifard* cannot render claim 2 unpatentable. For similar reasons, claim 3, which depends on claim 2, cannot be rendered unpatentable by *Abedifard*. Further, because *Abedifard* does not disclose or even suggest segments of memory cells, *Abedifard* does not disclose or even suggest segments of first and second sizes as recited in Claim 3. Therefore, it is respectfully submitted that Claims 2-3 are patentable over the references of record.

Claim 4 recites "the first plurality of memory cells stored said content therein as multilevel content, and said second plurality of memory cells store said content therein as a single level content." *Abedifard* does not disclose or even suggest multilevel memory cells and multilevel content. The Office Action does not cite where *Abedifard* allegedly discloses multilevel content and single level content. Applicant has performed a word search of "multilevel," and did not receive any hits in *Abedifard* for "multilevel." Lacking at least this

claim feature, *Abedifard* cannot render Claim 4 unpatentable. Therefore, it is respectfully submitted that Claim 4 is patentable over the references of record.

Claim 16-21 have been rejected under 35 U.S.C. § 102(b) as being anticipated by *Fung et al.* (U.S. Patent No. 6,215,685).

Claim 16 has been amended to recite in pertinent part "the segmented memory array including a plurality of memory cells arranged in segments and a plurality of tag bit cells.

As understood *Fung* at best merely discloses a volatile memory system that uses a content addressable memory 30 that includes a tag memory 20 and a data cache 29. (See Figure 6). *Fung* defines a tag as "any digital identifier (one or more bits) for data associated with the tag." ('685 Patent, col. 3, lines 3-5). The system uses the tag to determine whether to provide data. "When a target tag is matched to a tag in the CAM, the CAM provides the data associated with that tag." (*Id.* at lines 5-6).

Claim 16 has been amended to recite a memory array including memory cells arranged in segments. *Fung* does not disclose or even suggest segments of memory cells. Applicant has conducted a word search of *Fung* for the word "segment," and received no hits. Lacking at least this claim feature, *Fung* cannot render Claim 16 unpatentable.

Claim 17 recites "the memory cells store content therein as single level or multilevel content." The Office Action does not cite where *Fung* allegedly discloses multilevel content or single level content. Applicant has performed a word search of *Fung* for the word "multilevel," and received no hits. Thus, *Fung* does not disclose or even suggest multilevel memory cells and multilevel content. Lacking at least this claim feature, *Fung* cannot render Claim 17 unpatentable. Because Claims 18-19 depend directly on Claim 16, for similar reasons, *Fung* cannot render Claims 18-19 unpatentable.

Claim 20 recites "the tag bits are single level or multilevel." For similar reasons as Claim 17, *Fung* does not disclose or even suggest single level or multilevel tag bits. Because Claim 21 depends on Claim 20, for similar reasons, *Fung* cannot render Claim 20 unpatentable.

Therefore it is respectfully submitted that Claims 16-21 are patentable over the references of record.

Claims 22 and 25-28 have been rejected under 35 U.S.C. § 102(b) as being anticipated by *Nixon* (U.S. Patent No. 5,819,305).

Claim 22 has been amended merely to overcome the informalities of the objection described above.

As understood *Nixon* at best merely discloses an integrated circuit 10 that includes a memory 20 that is divided into a right memory array 60 and a left memory array 50. The sense amplifier 70 are coupled to a left column decode and select 56, which is coupled to the left memory array 50, and coupled to the right column decode and select 66, which is coupled to the right memory array 60. ('305 Patent, col. 2, lines 29-37). The "sense amplifier control circuit 72 provides control signals to sense amplifier 70 which control the configuration of memory 20, and the interaction of sense amplifier 70 with left memory array 50 and right memory array 60." (*Id.* at col. 4, lines 6-10"). The sense amplifier 70 may be operated in a referenced differential operating mode for a high density configuration of the memory 20. In this mode "the differential sense amplifiers compare bitline voltages to a voltage developed by a referenced current." (*Id.* at col. 4, lines 10-14). The sense amplifier 70 operate in a complimentary differential operating mode. The sense amplifier control circuit 72 "configures left memory array 50 and right memory array 60 into portions according to operating mode." (*Id.* at col. 4, lines 39-41). The reference differential operating mode and the complementary differential operating mode are operating modes that relate to the structure of the memory arrays 50 and 60 and not to the memory cells. In contrast, Claim 22 recites sensing modes to detect content of selected memory cells. Lacking at least this claim feature, *Nixon* cannot render Claim 22 unpatentable.

Because Claims 25-28 depend directly or indirectly on Claim 22, Nixon cannot render Claims 25-28 unpatentable. Therefore it is respectfully submitted that Claims 22 and 25-28 are patentable over the references of record.

Claims 60-62 and 64-66 have been rejected under 35 U.S.C. § 102(b) as being anticipated by *Shinkai* (U.S. Patent No. 6,381,190).

Claims 60 and 64 have been amended to recite a multimode sensing circuit.

As understood *Shinkai* at best merely discloses a data processing system that includes a control unit 50 with a CPU and a semiconductor memory device. Column 5, lines 3-11. The semiconductor memory device includes a memory cell array with a bank A and a bank B. See Figure 2. Each of the banks includes a sense amplifier section 2 and a memory cell array 1. Column 5, lines 18-20. There is no mention in *Shinkai* of a multimode sensing circuit. Further *Shinkai* does not disclose or even suggest "an interface controller to perform interface logic

depending on the selected memory array or depending on an external interface" as recited in Claim 60. The interface of *Shinkai* is an input/output buffer 5 with a latch circuit 6 under the control of a data control circuit 4. The interface of *Shinkai* does not perform interface logic depending on the selection of memory cell arrays bank A or bank B or on an external interface. Lacking at least this claim feature, *Shinkai* cannot render Claim 60 unpatentable. For similar reasons, Claims 61-62, which depend on Claim 60, cannot be rendered unpatentable by *Shinkai*.

For similar reasons Claims 64, which recites a multimode sensing circuit, and an IO driver controller, cannot be rendered unpatentable by *Shinkai*. For similar reasons, Claims 65-66, which depend on Claim 64, cannot be rendered unpatentable by *Shinkai*. Therefore it is respectfully submitted that Claims 60-62 and 64-66 are patentable over the references of record.

Claims 52-53 and 82 have been rejected under 35 U.S.C. § 102(e) as being anticipated by *Roohparvar* (U.S. Patent No. 6,657,899).

As understood *Roohparvar* at best merely discloses a memory device 100 that includes an array of flash memory cells 102. The array is arranged in four memory banks 104, 106, 108 and 110. Bank control logics 116, row address latch and decode circuitry 118 and row address multiplexer circuitry 114 are used for addressing the memory cells. Column 4, lines 25-38. "A read access to any bank can occur simultaneously with the background WRITE or ERASE operation to any other bank." Column 6, lines 41-43. *Roohparvar* does not disclose or even suggest "said first and second ones of the memory erase storing first and second type of content, respectively" as recited in Claim 52. The Office Action is silent as to where *Roohparvar* supposedly discloses such first and second type of content recited in Claim 52. Lacking at least this claim feature, *Roohparvar* cannot render Claim 52 unpatentable. Because Claim 53 depends on Claim 52, for similar reasons *Roohparvar* cannot render Claim 53 unpatentable.

Claim 82 recites "said first and second memory erase storing first and second type of content, respectively." For similar reasons described above in conjunction with Claim 52, *Roohparvar* cannot render Claim 82 unpatentable. Therefore it is respectfully submitted that Claims 52-53 and 82 are patentable over the references of record.

Claims 77 and 79 have been rejected under 35 U.S.C. § 102(e) as being anticipated by *Ha* (U.S. Patent No. 5,406,519).

Claims 77 and 79 have been amended to recite "a multi-mode sensing circuit to detect content of said selected ones of said first plurality of memory cells." As understood *Ha* at best

merely discloses a read only memory device that includes a security memory cell array 11 that includes a security code cell array for security code data. Column 3, lines 4-6. "If the external input data is coincident with the security code data in all addresses, the data stored in the storage cell array can be read during power-on and if not, regardless of power-on/off states, the data stored in the storage cell array can not be read." Column 3, lines 21-25. As understood the match of the security code of *Ha* is a match for all addresses, and not a security key stored for each array sector recited in Claims 77 and 79. Further, *Ha* does not disclose or even suggest a multi-mode sensing circuit to detect content of selected memory cells as recited in Claims 77 and 79. The sensing circuit of *Ha* does not have multiple modes. Lacking at least this claim feature, *Ha* cannot render Claims 77 and 79 unpatentable. Therefore it is respectfully submitted that Claims 77 and 79 are patentable over the references of record.

Claims 23-24 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nixon* in view of *Abedifard et al.*

Nixon and *Abedifard* are described above. It is noted in the Office Action that *Nixon* does not disclose memory cells arranged in segments or the segments of the first and second plurality of memory cells being a first size on the size, respectively. Contrary to the assertion in the Office Action that *Abedifard* discloses such segments, for the same reasons described above in conjunction with Claims 2 and 3, it is respectfully submitted that *Abedifard* does not disclose or even suggest segments of memory cells or segments of first and second sizes as recited in Claims 23 and 24. Neither *Nixon* nor *Abedifard*, either individually or in combination, disclose or even suggest the segments of memory cells or the segments of first and second sizes as recited in Claims 23-24. Lacking at least this claim feature, neither *Nixon* nor *Abedifard*, individually or in combination, can render Claims 23-24 unpatentable. Therefore it is respectfully submitted that Claims 23-24 are patentable over the references of record.

Claims 68-70 and 73-76 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Fung* et al.

Fung is described above. As noted above, Applicant has performed a word search of *Fung* for the word "multilevel" and received no hits. Thus, *Fung* does not disclose a "content addressable memory including a first plurality of multilevel memory cells" as recited in Claim 68. Lacking at least this claim feature, *Fung* cannot render Claim 68 unpatentable.

Because Claims 69-70 depend on Claim 68 either directly or indirectly, *Fung* cannot render Claims 69-70 unpatentable.

Claim 73 recites "the first plurality of memory cells being configurable to a number of memory levels." As noted above *Fung* does not disclose or even suggest multilevel memory cells. Lacking at least this claim feature, *Fung* cannot render Claim 73 unpatentable. Because Claims 74-76 depend directly or indirectly on Claim 73, for similar reasons *Fung* cannot render Claims 74-76 unpatentable. Therefore it is respectfully submitted that Claims 68-70 and 73-76 are patentable over the references of record.

Claim 83 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Roohparvar* in view of *Choate* (U.S. Patent No. 4,051,354).

Roohparvar is described above. *Choate* is cited for disclosing a plurality of monolithic arrays. Even assuming the combination of *Roohparvar* and *Choate* is proper, which Applicant does not concede, the combination of *Roohparvar* and *Choate* does not disclose or even suggest the "first and second memory arrays storing first and second type of content, respectively" as recited in Claim 83 for the reasons described above in conjunction with Claim 82. Lacking at least this claim feature, neither *Roohparvar* nor *Choate*, individually or in combination, can render Claim 83 unpatentable. Therefore it is respectfully submitted that Claim 83 is patentable over the references of record.

Claims 5-15, 29-36, 54-59, 63, 67, 71-72, 78, 80-81, and 84-85 have been objected to for being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. As noted above, amended claim 1, which is the base claim for claims 5-15, is submitted to be allowable. Thus for similar reasons, it is respectfully submitted that Claims 5-15 are allowable. As noted above, amended Claim 22, which is the base claim for Claims 29-36, is submitted to be allowable. Therefore for similar reasons, it is respectfully submitted that Claims 29-36 are allowable. As noted above, Claim 52, which is the base claim for Claims 54-59, submitted to be allowable. Thus for similar reasons, it is respectfully submitted that Claims 54-59 are allowable. Claims 63, 67, 78 and 80-81 have been rewritten in independent form, and therefore it is respectfully submitted that claims 63, 67, 78 and 80-81 are now allowable. As noted above, amended Claim 68, which is the base claim for Claims 71-72, is submitted to be allowable. Thus for similar reasons, it is respectfully submitted that Claims 71-72 are allowable.

As noted above, amended Claim 82, which is the base claim for Claims 84-85, is submitted to be allowable. Thus for similar reasons, it is respectfully submitted that Claims 84-85 are allowable.

The allowance of Claims 37-44 is noted. The preamble of Claims 37-44 has been amended merely for clarification. No new matter has been added. It is respectfully submitted that Claims 34-44 remain allowable.

Claims 86-90 have been added. It is respectfully submitted that new claims 86-90 are allowable for at least the reasons described above for the corresponding base claims.

It is respectfully submitted that the claims are in an allowable form, and action to that end is respectfully requested.

The Commissioner is hereby authorized to charge any fees which may be required, or credit in the overpayment, to Deposit Account No. 07-1896 referencing Attorney Docket No. **2102397-992830.**

Respectfully submitted,

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